Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently amended) A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising:

programming said programmable logic circuitry to function as communications port circuitry;

establishing with said programmed programmable logic circuitry a connection between said integrated circuit chip and an off-chip source of a data for use in reprogramming said programmable logic circuitry;

transferring said data from said off-chip source to said integrated circuit chip using said connection; and

using transferred data to reprogram said programmable logic circuitry to function as other than communications port circuitry.

2. (Previously presented) The method of claim 1 wherein said transferring data comprises transferring data from said off-chip source to a memory on said integrated circuit chip using said connection.

3. (Previously presented) The method of claim 1 wherein said programming comprises programming said programmable logic circuitry to function as Ethernet media access controller (MAC) circuitry.

4. (Previously presented) The method of claim 1 further comprising before said programming:

establishing a first connection between said integrated circuit chip and a first off-chip source of data for use in programming said programmable logic circuitry to function as communications port circuitry; and

transferring data for use in programming said programmable logic circuitry to function as communications port circuitry from said first off-chip source to said integrated circuit chip using said first connection.

5. (Previously presented) The method of claim 4 wherein said establishing a first connection comprises establishing with Ethernet MAC circuitry a first connection between said integrated circuit chip and a first off-chip source of data for use in programming said programmable logic circuitry to function as communications port circuitry.

6. (Currently amended) A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising:

establishing with receiver/transmitter circuitry a first connection between said integrated circuit chip and ~~an~~ a first off-chip source of first data;

transferring said first data from said first off-chip source to said integrated circuit chip using said first connection;

programming Ethernet media access controller (MAC) circuitry with said transferred first data;

establishing with said Ethernet MAC circuitry a second connection between said integrated circuit chip and a second off-chip source of second data;

transferring said second data from said second off-chip source to said integrated circuit chip using said second connection; ~~and~~

using said transferred second data from said second off-chip source to program said programmable logic circuitry; and

operating the integrated circuit chip to break at least one of said first and second connections after that connection has been used in the transferring of data.

7. (Currently amended) The method of claim 6 wherein said programming Ethernet MAC circuitry comprises programming Ethernet MAC circuitry with said transferred first data indicating a speed of operation at which said Ethernet MAC circuitry is to operate.

8. (Currently amended) A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising:

establishing with receiver/transmitter circuitry a first connection between said integrated circuit chip and ~~an~~ a first off-chip source of first data;

transferring said first data from said first off-chip source to said integrated circuit chip using said first connection;

programming said programmable logic circuitry with said transferred first data to function as Ethernet media access controller (MAC) circuitry;

establishing with said programmed programmable logic circuitry a second connection between said integrated circuit chip and a second off-chip source of second data;

transferring said second data from said second off-chip source to said integrated circuit chip using said second connection; and

using said transferred second data to reprogram said programmable logic circuitry to function as something other than said Ethernet MAC circuitry.

9. (Currently amended) An integrated circuit chip comprising:

programmable logic circuitry;

processor circuitry operative to program said programmable logic circuitry; and

Ethernet media access controller (MAC) circuitry ~~operative to establish a connection between said chip and an off-chip source of data, said Ethernet MAC circuitry~~ coupled to said processor circuitry, said Ethernet MAC circuitry being operative to establish a connection between said integrated circuit chip and an off-chip source of a data so that said data from said off-chip source can be brought into said integrated circuit chip via said connection, after which said Ethernet MAC circuitry is operative to sever said connection, said processor circuitry being operative to program said programmable logic with said data brought into said integrated circuit chip via said connection for operation of said integrated circuit chip after said connection has been severed.

10. (Previously presented) The integrated circuit chip of claim 9 wherein said processor circuitry is microprocessor circuitry.

11. (Previously presented) The integrated circuit chip of claim 9 wherein said programmable logic circuitry is reprogrammable.

12. (Previously presented) An end-user system comprising:

a circuit board comprising:

a processor;

a memory;

I/O circuitry;

an integrated circuit chip as defined in claim 9; and

a system bus coupling said processor, memory, I/O circuitry, and integrated circuit chip.

13. (Previously presented) The end-user system of claim 12 further comprising a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

14. (Previously presented) The end-user system of claim 12 wherein said circuit board further comprises a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

15. (Previously presented) The end-user system of claim 12 wherein said end-user system comprises a data processing system.

16. (Previously presented) A circuit board on which is mounted an integrated circuit chip as defined in claim 9.

17. (Currently amended) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as communications port circuitry;

processor circuitry operative to program said programmable logic circuitry;

memory circuitry;

Ethernet media access controller (MAC) circuitry operative to establish a connection between said integrated circuit chip and an off-chip source of a data to

bring said data for programming the programmable logic circuitry into the integrated circuit chip from the off-chip source via the connection, after which the Ethernet MAC circuitry severs the connection; and

interconnection bus circuitry coupled to said programmable logic circuitry, processor circuitry, memory circuitry, and Ethernet MAC circuitry.

18. (Previously presented) The integrated circuit chip of claim 17 wherein said processor circuitry comprises a central processor unit.

19. (Previously presented) The integrated circuit chip of claim 17 wherein said processor circuitry is microprocessor circuitry.

20. (Previously presented) The integrated circuit chip of claim 17 wherein said memory circuitry is random access memory (RAM).

21. (Previously presented) An end-user system comprising:

a circuit board comprising:

a processor;

a memory;

I/O circuitry;

an integrated circuit chip as defined in claim 17; and

a system bus coupling said processor, memory, I/O circuitry, and integrated circuit chip.

22. (Previously presented) The end-user system of claim 21 further comprising a source of configuration data for said programmable logic circuitry, said integrated

circuit chip operative to establish a connection to said source.

23. (Previously presented) The end-user system of claim 21 wherein said circuit board further comprises a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

24. (Previously presented) The end-user system of claim 21 wherein said end-user system comprises a data processing system.

25. (Previously presented) A circuit board on which is mounted an integrated circuit chip as defined in claim 17.

26. (Currently amended) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as communications port circuitry;

processor circuitry operative to program said programmable logic circuitry to establish a first connection between said integrated circuit chip and an off-chip source of first data for configuring said integrated circuit chip for first further operations, after which the programmable logic circuitry severs the first connection;

receiver/transmitter circuitry;

Ethernet media access controller (MAC) circuitry operative to establish a second connection between said integrated circuit chip and an off-chip source of second data for configuring the programmable logic circuitry for second further operations, after which the Ethernet MAC circuitry severs the second connection; and

interconnection bus circuitry coupled to said programmable logic circuitry, processor circuitry, receiver/transmitter circuitry, and Ethernet MAC circuitry.

27. (Previously presented) The integrated circuit chip of claim 26 wherein said programmable logic circuitry is operative to be selectively reprogrammed.

28. (Previously presented) The integrated circuit chip of claim 26 further comprising memory circuitry wherein said processor circuitry is operative to program said programmable logic circuitry with data stored in said memory circuitry.

29. (Previously presented) The integrated circuit chip of claim 26 wherein said memory is a random access memory (RAM).

30. (Previously presented) An end-user system comprising:

a circuit board comprising:

a processor;

a memory;

I/O circuitry;

an integrated circuit chip as defined in claim 26; and

a system bus coupling said processor, memory, I/O circuitry, and integrated circuit chip.

31. (Previously presented) The end-user system of claim 30 further comprising a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

32. (Previously presented) The end-user system of claim 30 wherein said circuit board further comprises a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

33. (Previously presented) The end-user system of claim 30 wherein said end-user system comprises a data processing system.

34. (Previously presented) A circuit board on which is mounted an integrated circuit chip as defined in claim 26.

35. (Currently amended) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as Ethernet media access controller (MAC) circuitry for establishing a connection between said integrated circuit chip and an off-chip source of a data to bring said data for further programming the programmable logic circuitry into the integrated circuit chip from the off-chip source via the connection, after which the programmable logic circuitry severs the connection;

processing circuitry operative to program said programmable logic circuitry;

receiver/transmitter circuitry; and

interconnection bus circuitry coupled to said programmable logic circuitry, processing circuitry, and receiver/transmitter circuitry.

36. (Previously presented) An end-user system comprising:

a circuit board comprising:

a processor;

a memory;

I/O circuitry;

an integrated circuit chip as defined in claim 35; and

a system bus coupling said processor, memory, I/O circuitry, and integrated circuit chip.

37. (Previously presented) The end-user system of claim 36 further comprising a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

38. (Previously presented) The end-user system of claim 36 wherein said circuit board further comprises a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

39. (Previously presented) The end-user system of claim 36 wherein said end-user system comprises a data processing system.

40. (Previously presented) A circuit board on which is mounted an integrated circuit chip as defined in claim 35.